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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,323	12/05/2003	Kenneth J. Goodnow	BUR920020125US1	1322

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EXAMINER
DOAN, NGHIA M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/707,323	GOODNOW ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13, 16-19, 22-26, and 28* is/are rejected.

7)☒ Claim(s) *14-15, 20-21, and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/707,323 filed on 12/05/2003 and Applicant's argument filed on 01/26/2006, claims 9-28 are pending.

Claims 25-27 have been amended.

The claim Objection is obviated.

2. Applicant's arguments, see page 6, Applicant indicate the limitation "the step of disabling", which is supported by the application specification, with respect to claims 15 and 21 have been fully considered and are persuasive. The Claims Rejection under 35 U.S.C 112, first paragraph in the last Office Action has been withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-13, 16-19, 22-26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiefele et al. (Schiefele) (US 6,526,559).

5. **With respective to claims 9, 16, and 23,** Schiefele teaches a method and system for creating circuit redundancy in programmable logic device (abstract and col. 1, ll. 16-27), comprising the steps of:

(as per claims 9, 16, and 23) (means for) creating an integrated circuit design description using a hardware designed language (HDL) (col. 13, ll. 44-48);

(as per claims 9, 16, and 23) (means for) adding a fault tolerant operator (virtual redundancy) to the particular logic functions in said integrated circuit design description (col. 1, ll. 14-15 and col. 13, ll. 49-67);

(as per claims 16 and 23) (means for) synthesizing (compiling) said integrated circuit design description after said means for adding step (figure 18, steps [260-280]), col. 13, ll. 49-67, and col. 14, ll. 12-32); and

(as per claims 9, 16, and 23) (means for) building redundant copies for the particular logic function having a fault tolerant operator (virtual redundancy) (col. 5, ll. 32-50, col. 6, ll. 15-43, col. 12, ll. 12-20, and col. 14, ll. 12-32).

Schiefele creating an integrated circuit description using an HDL, but Schiefele does not specifically indicated that using an HDL at the Register-transfer level (RTL). However, a circuit description using an HDL at the register transfer level is well-known in the art.

6. **With respective to claims 10, 22 and 28,** Schiefele teaches all the limitations of set forth claims, wherein said integrated; circuit design description in said creating step is for a FPGA (Abstract and col. 1, ll. 7-45).

7. **With respective to claims 11, 17, and 24,** Schiefele teaches all the limitations of set forth claims, wherein said building step includes building at least three physical copies of each logic function having a fault tolerant operator (col. 10, ll. 37-49 and col. 11, ll. 24-27).

8. **With respective to claims 12, 18 and 25,** Schiefele teaches all the limitations of set forth claims, further comprising the step of determining which of said at least three physical copies is faulty (col. 4, ll. 59-67 and col. 5, ll. 1-12).

9. **With respective to claims 13, 19, and 26,** Schiefele teaches all the limitations of set forth claims, wherein said step of determining includes using a majority voter (col. 1, ll. 35-38, col. 4, ll. 11-12, col. 9, ll. 56-67, and col. 10, ll. 63-65).

Allowable Subject Matter

10. Claims 14-15, 20-21 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the prior of made record does not teach or fairly suggest the method of building faulty tolerant logic function in an integrated circuit comprising the inventive step of (as per claims 14, 20 and 27) receiving at said majority voter an output value from each of said at least three physical copies of each logic function, wherein for any minority output value at said majority voter, said respective copy is deemed faulty; and (as per claims 15 and 21) disabling any of said at least three physical copies that are faulty.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

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